REMARKS

It is initially noted that the Board ordered on September 28, 2006 that this application be handled with "special dispatch" on page 16 of their Decision on Appeal. This application has been pending for almost ten years and more than ten years when considering the provisional application. It is therefore requested that the order of the Board be honored.

The following meets the provisions of 37 C.F.R. 41.202(a)(1)-(6) as required in the Office action and by the Board:

It is initially noted that the REMARKS in the papers mailed to the Patent and Trademark Office on or about November 6, 2001 and on or about July 24, 2002 and the Declaration of the applicants filed on or about November 15, 2001are pertinent since those REMARKS and Declaration provide substantially all of what is required by the above-noted C.F.R. sections. Those REMARKS and Declaration are incorporated herein by reference and are of record. It follows that everything required by the above-noted section has been of record for more than five years. The following is a recapitulation of what is of record.

Claims 22 to 31 are substantially identical to claims 1 to 8, 10 and 11 respectively of Potter Patent No. 6,028,437 and are copied from Potter except as noted below as to claim 22.

With regard to sections (a)(1)-(6) of section 41.202:

Claim 22 above is the same as claim 1 of Potter except that the terms used in the subject application "interconnecting medium" have been used in place of the term --probe membrane-- and "medium surface" has been used in place of the term --probe membrane

head--. This readability should be sufficient to provide a first count (claim 9 of the subject application can also be used as an additional or alternate count) for purposes of interference with all other claims coming under the count or counts. Claim 22, which is essentially the same as claim 1 of Potter except as noted above, is therefore readable on the subject disclosure as follows with the bracketed words being those used in Potter as follows:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1); and

an interconnecting medium (140) [probe membrane] contained within said package having electrical paths (171-173) adaptable for coupling to test circuitry, wherein said interconnecting medium [probe membrane] includes a medium surface (top surface of 140 in Fig. 1b) [probe membrane head], a plurality of standoffs (13 of Fig. 3) affixed to said medium surface [probe membrane], and a plurality of probe tips (11 of Fig. 3) affixed to said medium surface [probe membrane head], said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips.

Claim 9 is readable on Potter as follows:

9. An interconnecting layer for use in a semiconductor package which comprises;

(a) an electrically insulating layer (121 of Potter);

(b) electrically conductive paths on said layer (traces not shown but discussed at column 3, lines 45 to 57), each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump (122) having a height greater than all other structures on said layer; and

(c) a standoff (123) disposed on said layer and having a height above said layer and less than said bump.

With reference to the remaining claims of Potter, these claims would come in under the count, whether or not they can be made in the subject application. Accordingly, the interference should be declared just on the basis of the readability of claims 22 and 9 on the Potter patent. Under the interference Rules, additional claims can be added to come under the count in the Motion period.

With reference to claim 23, this claim is readable on the subject disclosure as follows:

said package (110) further comprising: a package base having an upper surface adapted (base of cavity 112) to receive said interconnecting medium (140), said medium having a medium lower surface (lower surface of 140);

a bonding layer interposed between said medium lower surface and said package base upper surface (120 and 135); and

a package lid (160) having a lower surface adapted to receive said semiconductor device, wherein said package lid is positioned above said package base.

With reference to claim 24, the claim is readable on the subject disclosure as follows:

said bonding layer (120 and 135) is comprised of an elastomeric material.

With reference to claim 25, the claim is readable on the subject disclosure as follows:

said semiconductor device is a die (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claim 26, the claim is readable on the subject disclosure as follows:

said semiconductor device is a wafer (130) having an upper surface, said upper surface fixed to said package lid lower surface by a bonding layer interposed therebetween (140 and 150).

With reference to claims 27 and 28, these claims are readable on the subject disclosure as follows:

said bonding layer interposed between said die and said package lid lower surface is comprised of an elastomeric material (page 9, line 11).

With reference to claim 29, this claim is readable on the subject disclosure as follows:

the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

With reference to claim 30, this claim is readable on the subject disclosure as follows:

An apparatus adaptable for the testing of semiconductor devices comprising:

a package (110 of Fig. 1), wherein said package has a package lid (160) having a lower surface adapted for receiving said semiconductor device, said semiconductor device (130) having an upper surface, and a package base having an upper surface (112);

an interconnecting medium (140) contained within said package, wherein said interconnecting medium has electrical paths (171, 172, 173) adaptable for coupling to test circuitry, said medium including a medium surface, said medium surface having a plurality of probe tips (11) affixed thereto, a plurality of standoffs (13) affixed thereto, and a lower surface, wherein said probe tips are adaptable for making electrical contact with pads (135) on said semiconductor device (130) and are compliant bump probe tips (sentence bridging pages 9 and 10);

a bonding layer (120, 135) comprising an elastomeric material (page 9, line 11) interposed between said package lid lower surface and said semiconductor device upper surface; and

a bond layer (140, 150) comprising an elastomeric material interposed between said interconnecting medium lower surface and said package base upper surface, said package base being adapted for receiving said interconnecting medium.

With reference to claim 31, this claim is readable on the subject disclosure as follows:

the compliant bump probe tips are comprised of a solid material (see, for example, Patent No. 5,508,228 cited at page 11, line 15).

The applicants will prevail on priority for several reasons. First, the applicants provided the invention to the assignee of Potter (Diamond Tech One, hereinafter DTO) under a non-disclosure agreement for the purposes of having DTO provide their membrane as stated in the invention disclosure attached to the Declaration filed by the inventors on or about November 15, 2001. Furthermore, the invention disclosure above mentioned is dated prior to the filing date of Potter and establishes the fact that the

applicants herein not only made the invention listed in the claims and proposed accounts set forth above, but further that the invention was initially communicated by applicants herein to DTO (Potter). This is fully set forth therein in the paragraph on page 2 relative to Figure 3 and in the section entitled "Interconnecting Medium" of the invention disclosure.

Claim 22 is readable on the invention disclosure as follows:

22. An apparatus adaptable for the testing of semiconductor devices comprising:

a package (Fig. 3 of invention disclosure); and

an interconnecting medium contained within said package having electrical paths adaptable for coupling to test circuitry (370 of Fig. 3 and 476 of Fig. 4), wherein said interconnecting medium includes a medium surface (surface of 370 and 476), a plurality of standoffs affixed to said medium surface (474 of Fig. 4), and a plurality of probe tips affixed to said medium surface, said probe tips adaptable for making electrical contact with pads on said semiconductor device, wherein said probe tips are compliant bump probe tips (47 1, 472 and 475 of Fig. 4).

Claim 9 is readable on the invention disclosure as follows:

9. An interconnecting layer for use in a semiconductor package (Fig. 3) which comprises;

(a) an electrically insulating layer (substrate of 370 and 476);

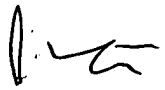
(b) electrically conductive paths on said layer (473 of Fig. 4), each of said paths having first and second spaced apart regions thereon, said second spaced apart region of each of said paths having a compliant bump having a height greater than all other

structures on said layer (371, 372, 471, 472, 475 and discussion under "Interconnecting Medium of invention disclosure); and

(c) a standoff disposed on said layer and having a height above said layer and less than said bump (474 and discussion under "Interconnecting Medium" of invention disclosure).

In view of the above showing and the papers already of record, all requirements of the Office action have been met. Accordingly, it is requested that the interference be declared forthwith.

Respectfully submitted,



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